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REMARKS

By the foregoing Amendment, the specification has been amended, Claims 1 and 9 to 23 have been canceled, and new Claims 24-28 have been added. A marked up version of showing the changes made is attached. Favorable reconsideration of the application is respectfully requested.

The Examiner objected that the specification did not mention Fig. 3. However, the Examiner's attention is directed to the specification at page 6, lines 8-9 which describes Fig. 3. The specification has been corrected at pages 10, 18 and 31 in accordance with the Examiner's suggestions. It is thus believed that the Examiner's objections to the specification have now been overcome.

Claim 1 was rejected under the judicially created doctrine of obviousness-type double patenting in view of Claim 1 of U.S. Patent No. 6,157,384. Claim 1 has now been canceled, so that it is believed that this rejection can be withdrawn.

Claims 5-8 were rejected under 35 U.S.C. 103(a) on the grounds of obviousness from Ohba, U.S. Patent No. 6,362,827. Ohba claimed priority from PCT/JP97/00298 filed February 6, 1997. The present application claims priority from PCT/JP97/00297 filed February 6, 1997, which claimed priority from Japanese Patent

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Application P8-020332 filed February 6, 1996, and the specification has been amended to clarify this fact. The claim for priority was presented upon the filing of the application on August 1, 2000. It is therefore believed that U.S. Patent No. 6,362,827 is not prior art to the present application, and that application of the reference in the rejection of the claims of the present application under 35 U.S.C. 103(a) on the grounds of obviousness should be withdrawn.

Claims 9, 17, 10-16 and 18-23 were rejected under 35 U.S.C. 112, second paragraph, on the grounds of indefiniteness. Claims 9-23 have been canceled, and new claims 24-28 have been added, so that it is believed that this rejection can now be withdrawn.

It is believed that no fee is due in connection with this matter. However, should a fee be required, the Commissioner is authorized to charge any fee due in connection with this matter to Deposit Account No. 06-2425.

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In light of the foregoing, it is respectfully submitted that the application should now be in a condition for allowance, and an early favorable action in this regard is respectfully requested.

Respectfully submitted,

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DGP/rvw

Encls.: Version With Markings To Show Changes Made
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

At page 1, the "Related Applications:" paragraph is changed to read as follows:

Related Applications:

This is a continuation of Serial No. 08/930,648 filed January 20, 1998, now
Patent No. 6,157,384. This application claims priority from PCT/JP97/00297 filed
February 6, 1997, which claimed priority from Japanese Patent Application P8-020332
filed February 6, 1996.

At page 10, line 18 to 23, the paragraph is changed to read as follows:

The [CPU] GPU 15 is a device on the main bus 1 functioning as a rendering processor. This GPU 15 interprets the drawing command sent from the main CPU 11 or main DMAC 13 as a command packet and performs rendering processing of writing pixel

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data in the frame buffer 18 from Z-values specifying depth and color data of all pixels making up a polygon.

The paragraph from page 17, line 20, to page 18, line 6 is changed to read as follows:

The data structure in the texture cache 33F, shown as an example in Fig. 4, is comprised of a tag area TAG made up of texture addresses, a storage area DATA having stored therein the necessary texture data and a flag L specifying that the texture data has not as yet been used. For employing the entry, having the flag L reset, the texture cache 33F reads in the texture data from the texture area of the frame buffer 18 to set its flag L. The drawing engine 33 reads out the corresponding texture data from the entry, the flag of which has been set, in order to perform drawing processing, and resets the flag [1] L of the entry at a stage in which the drawing has come to a close and hence the texture data is no longer required.

The paragraph from page 30, line 25, to page 31, line 8 is changed to read as follows:

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If fed with the mask information from the control circuit 101, the selector 102 designates for MUX/DMUX [111103a] 103a to 103d the accessing addresses obtained as a result of masking performed in the (4x4) interleaving patterns P, on the basis of the masking information, as shown in Fig. 9. Thus, of the addresses A_0 to A_{15} in the interleaving pattern specified by P(4,1) shown in Fig. 9, the addresses to be accessed, obtained as the result of masking, are A4, A5, A6, A8, A9, A10, A13, A14 and A15, shown shaded in Fig. 10.